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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/581,528	02/07/2007	Hitoshi Tsuge	292022US2PCT	9466

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EXAMINER	
SHERMAN, STEPHEN G	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/581,528	TSUGE, HITOSHI	
	Examiner	Art Unit	
	STEPHEN G. SHERMAN	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *69,70 and 72-77* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *69,70 and 72-77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *7 February 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed 9 December 2010. Claims 69, 70 and 72-77 are pending.

Response to Arguments

2. Applicant's arguments with respect to claims 69, 70 and 72-77 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 69, 70, 72, 73 and 75-77 are rejected under 35 U.S.C. 103(a) as being unpatentable over Numao (US 2003/0011314) in view of Tsuruoka et al. (US 6,414,443).

Regarding claim 69, Numao discloses a self-luminescent display apparatus comprising:

self-luminescent elements arranged in a pattern of a matrix (Figure 1, 2);

driving transistors, each of which controls a current supplied to each of said self-luminescent elements (Figure 1, each pixel A11 has a driving TFT shown as Q2 in Figure 2.);

pixel circuits provided in association with each of said self-luminescent elements and each of said driving transistors (Figure 1, A11); and

a voltage generation section to supply a gradation voltage, which is to correspond to a display grade, to said driving transistors (Figure 1, 4),

wherein a gate voltage of each of said driving transistors changes due to the changed gradation voltage supplied from said voltage generation section (Figures 1 and 2, and paragraphs [0073], [0075] and [0079], where a change in voltage to the data lines D1-Dn will change the voltage at the gate of Q2.).

Numao fails to explicitly teach wherein the gradation voltage is supplied such that the sum of currents flowing through said self-luminescent elements is a predetermined current value.

Tsuruoka et al. disclose a self-luminescent display apparatus comprising:

a voltage generation section to supply a gradation voltage, which is to correspond to a display grade, to pixels of the display (Figure 4, 34. See column 5, lines 50-54.),

wherein the gradation voltage is supplied such that the sum of currents flowing through said self-luminescent elements is a predetermined current value (Figure 3 and column 5, line 65 to column 6, line 37 and column 6, line 64 to column 7, line 2.).

Therefore, it would have been obvious to “one of ordinary skill” in the art at the time the invention was made to use the teachings of Tsuruoka et al. in the self-luminescent display apparatus taught by Numao such that the sum of currents flowing through said self-luminescent elements is a predetermined current value in order to obtain enhanced display quality (Tsuruoka et al., column 6, lines 35-37).

Regarding claim 70, please refer to the rejection of claim 69, and furthermore Tsuruoka et al. also discloses where the voltage outputted from said voltage generating section is changed according to temperature (Figures 2B and 4 and column 5, line 24 to column 6, line 25).

Regarding claim 72, Numao, Tsuruoka et al. and Abe disclose the self-luminescent display apparatus according to Claim 69.

Tsuruoka et al. also disclose wherein said voltage generation section adjusts the gradation voltage such that when the gradation voltage is supplied to said pixels, the sum of currents flowing through said self-luminescent elements is measured and adjusted to be the predetermined current value (Figure 3 and column 5, line 65 to column 6, line 37 and column 6, line 64 to column 7, line 2. [where in combination the gradation voltage would be supplied to the driving transistors]).

Regarding claim 73, Numao, Tsuruoka et al. and Abe disclose the self-luminescent display apparatus according to Claim 69.

Numao also discloses the apparatus further comprising:

an adjustor circuit to adjust the gradation voltage generated by said voltage generation section (Figure 1, K1-Kn, M1-Mn and B1-Bn act as the adjuster circuit.), and

a memory unit to store a voltage value set by said adjustor circuit (Figure 2, capacitor C1 is a memory unit which will store the voltage.).

Regarding claim 75, Numao, Tsuruoka et al. and Abe disclose the self-luminescent display apparatus according to Claim 69.

Tsuruoka et al. also disclose the apparatus further comprising:

a temperature compensation unit to generate a signal inputted to said voltage generation section according to the change of ambient temperature, wherein the gradation voltage outputted from said voltage generation section is changed by the signal inputted from said temperature compensation unit, thereby to compensate for a temperature characteristic of the currents flowing through said self-luminescent elements (Figure 2b and 4, 35 and column 5, line 38 to column 6, line 24.).

Regarding claim 76, Numao, Tsuruoka et al. and Abe disclose the self-luminescent display apparatus according to Claim 69.

Numao also discloses wherein said voltage generation section comprises at least one predetermined circuit including said driving transistor and a storage capacity, disposed in said pixel circuit, and the gradation voltage is generated based on a gate voltage or drain voltage of said driving transistor (Figure 2 shows that driving transistor Q2 and capacitor C1 are part of the "voltage generation section" since they receive the voltage from the variable power supply and then generate the driving of the OLED P.).

Regarding claim 77, Numao, Tsuruoka et al. and Abe disclose the self-luminescent display apparatus according to Claim 76.

Numao also discloses wherein at least two predetermined circuits including said driving transistor and a storage capacity (Figure 2), respectively, are provided, and one of said predetermined circuits is selected and used as said voltage generation section (Figure 2, where one of the circuits will be selected in the first row when the gate signal is high, and then the pixel circuit will be used to generate the voltage as shown in Figures 1 and 2. Thus one of the circuits will be selected and used as said voltage generation section.).

5. Claim 74 is rejected under 35 U.S.C. 103(a) as being unpatentable over Numao (US 2003/0011314) in view of Tsuruoka et al. (US 6,414,443) and further in view of Kasai (US 6,989,826).

Regarding claim 74, Numao and Tsuruoka et al. disclose the self-luminescent display apparatus according to Claim 69.

Numao and Tsuruoka et al. fail to teach wherein the display grade corresponds to a grade of black display

Kasai discloses a self-luminescent display apparatus wherein a display grade applied to the pixels corresponds to a grade of black display (Figure 18 and column 15, lines 1-24).

Therefore, it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the teachings of applying a pre-charge signal according to a black display grade as taught by Kasai in the self-luminescent display apparatus taught by the combination of Numao and Tsuruoka et al. in order to shorten the driving time of the data lined used in the unit circuits (Kasai, column 1, lines 54-55).

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEPHEN G. SHERMAN whose telephone number is (571)272-2941. The examiner can normally be reached on M-F, 7:30 a.m. - 4:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Stephen G Sherman/
Primary Examiner, Art Unit 2629

4 January 2011